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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,887	08/10/2004	Meng-Chi Liu	CPTP0002USA	4886

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EXAMINER	
CHEN, WEN YING PATTY	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/710,887	LIU ET AL.	
	Examiner	Art Unit	
	W. Patty Chen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuda et al. (US 2002/0015126).

With respect to claim 1: Tsuda et al. disclose in Figure 5C a multi-domain vertical alignment (MVA) LCD panel, comprising:

a first substrate (Figure 2, element 1) having a plurality of pixel regions arranged in arrays;

a second substrate (Figure 2, element 27) positioned parallel to and directly above the first substrate;

a plurality of common lines (Figure 1, elements 8 and 9) positioned on a surface of the first substrate facing the second substrate, each common line traversing corresponding pixel regions;

a plurality of pixel electrodes (element 12) respectively positioned in each pixel region and above the common lines (Paragraph 0026; wherein the common lines are formed the same layer as the gate lines), each pixel electrode comprising a plurality of slits (element 17C);

a dielectric layer positioned between the common lines and the pixel electrodes (as shown in Figure 2 and described in Paragraphs 0026-0028);

a liquid crystal layer (Figure 2, element 29) positioned between the first substrate and the second substrate;

a common electrode (element 54) positioned on a surface of the second substrate facing the first substrate; and

a plurality of protrusions (element 18) positioned on a surface of the common electrode layer, each protrusion being arranged parallel to and alternately with each slit (as shown in Figure 1), the protrusions and the common lines positioned in the pixel regions being partially overlapped (as shown in Figure 1).

As to claim 9: Tsuda et al. further disclose in Figure 1 that each common line in each pixel region forms an H-shaped electrode pattern comprising a first electrode pattern (element 8) and two second electrode patterns (element 9), the first electrode pattern traversing a middle of each pixel region, and the two second electrode patterns being perpendicular to the first electrode pattern.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 2004/0095538).

With respect to claim 1: Kim et al. disclose in Figures 4B and 5 a multi-domain vertical alignment (MVA) LCD panel, comprising:

a first substrate (element 31) having a plurality of pixel regions arranged in arrays;

a second substrate (element 33) positioned parallel to and directly above the first substrate;

a plurality of common lines (element 15) positioned on a surface of the first substrate facing the second substrate, each common line traversing corresponding pixel regions;

a plurality of pixel electrodes (element 13) respectively positioned in each pixel region and above the common lines, each pixel electrode comprising a plurality of slits (element 51);

a dielectric layer (element 37) positioned between the common lines and the pixel electrodes;

a liquid crystal layer (not labeled) positioned between the first substrate and the second substrate;

a common electrode (element 17) positioned on a surface of the second substrate facing the first substrate; and

a plurality of protrusions (element 53) positioned on a surface of the common electrode layer, each protrusion being arranged parallel to and alternately with each slit (as shown in Figure 4B), the protrusions and the common lines positioned in the pixel regions being partially overlapped (as shown in Figure 4B).

As to claim 2: Kim et al. further disclose in Figure 5 that the MVA LCD panel further comprising a color filter layer (element 23) positioned between the second substrate and the common electrode layer.

As to claim 3: Kim et al. further disclose in Figure 5 that the MVA LCD panel further comprising a black matrix layer (element 25) positioned on the surface of the second substrate

facing the first substrate, and corresponding to areas outside of each pixel region of the first substrate.

As to claim 4: Kim et al. further disclose in Paragraph 0053 that the common lines are electrodes of storage capacitors.

As to claim 5: Kim et al. further disclose in Figure 4B that the MVA LCD panel further comprising a plurality of thin film transistors (TFTs) positioned in each pixel region.

As to claim 6: Kim et al. further disclose in Figure 4B that the MVA LCD panel further comprising a plurality of data lines (element 3) electrically connected to a source of each thin film transistor.

As to claim 7: Kim et al. further disclose that the common lines serve as dummy circuits while the data lines are disconnected (since the common lines are overlapped with the data lines, thus have the function of serving as dummy circuits while the data lines are disconnected).

As to claim 8: Kim et al. further disclose in Figure 4B that the critical dimensions of the protrusions (element 53) are less than those of the common lines.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kida et al. (US 2004/0041976) in view of Tsuda et al. (US 2002/0015126).

With respect to claim 10: Kida et al. disclose in Figures 5 and 6 a multi-domain vertical alignment (MVA) LCD panel, comprising:

a first substrate (element 11) having a plurality of pixel regions arranged in arrays;

a second substrate (element 21) positioned parallel to and directly above the first substrate;

a plurality of electrode patterns comprising a first electrode pattern (element 11b);

a plurality of pixel electrodes (element 16) respectively positioned in each pixel region and above the electrode patterns, each pixel electrode comprising a plurality of slits (element 16a) not overlapping the first electrode pattern (element 11b);

a dielectric layer (element 12) positioned between the common lines and the pixel electrodes;

a liquid crystal layer (element 30) positioned between the first substrate and the second substrate;

a common electrode layer (element 23) positioned on a surface of the second substrate facing the first substrate; and

a plurality of protrusions (element 24) positioned on a surface of the common electrode layer, each protrusion being arranged parallel to and alternately with each slit (as shown in Figure 5), the protrusions and each first electrode pattern (element 11b) being overlapped.

Kida et al. fail to disclose that the electrode patterns being H-shaped and further comprising two second electrode patterns wherein the first electrode pattern traversing a middle of the ach pixel region, and the two second electrode patterns are perpendicular to the first electrode pattern.

However, Tsuda et al. disclose in Figure 1 a multi-domain vertical alignment (MVA) LCD panel comprising electrode patterns formed in H-shaped wherein the first electrode pattern (element 8) traversing a middle of the ach pixel region, and two second electrode patterns (element 9) are perpendicular to the first electrode pattern.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a MVA LCD panel as taught by Kida et al. wherein the

electrode patterns formed in H-shaped such that the first electrode pattern traversing a middle of the ach pixel region, and two second electrode patterns are perpendicular to the first electrode pattern as taught by Tsuda et al., since Tsuda et al. teach that by forming the capacitance lines into such a shape having the two branch electrodes formed in the edge portions of the pixel electrode serves as auxiliary capacitance to the pixel and helps to decrease the potential change in the pixel electrode (Paragraphs 0029-0030)

As to claim 11: Kida et al. further disclose in Figure 6 that the MVA LCD panel further comprising a color filter layer (element 22) positioned between the second substrate (element 21) and the common electrode layer (element 23).

As to claim 12: Kida et al. further disclose Paragraph 0042 that the MVA LCD panel further comprising a black matrix layer (formed by overlapping the color filter layers of different colors) positioned on the surface of the second substrate facing the first substrate, and corresponding to areas outside of each pixel region of the first substrate.

As to claim 13: Tsuda et al. further disclose in Paragraphs 0029-30 that the common lines are electrodes of storage capacitors.

As to claim 14: Tsuda et al. further disclose in Paragraphs 0029-30 that the electrode patterns are electrically connect to one another.

As to claim 15: Kida et al. further disclose in Figure 5 that the MVA LCD panel further comprising a plurality of thin film transistors (TFTs) (element 14) positioned in each pixel region, and a plurality of data lines (element 13) electrically connected to a source of each thin film transistor.

As to claim 16: Tsuda et al. further disclose in Figure 1 that the common lines (elements 8 and 9) serve as dummy circuits while the data lines (element 7) are disconnected (since the common lines are overlapped with the data lines, thus have the function of serving as dummy circuits while the data lines are disconnected).

As to claim 17: Kida et al. further disclose in Figure 5 that the critical dimensions of the protrusions (element 24) are less than those of the common lines (element 11b).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. Patty Chen whose telephone number is (571)272-8444. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

W. Patty Chen
Examiner
Art Unit 2871

WPC
6/02/06

ANDREW SCHECHTER
PRIMARY EXAMINER